WHAT IS CLAIMED IS:

1. An integrated semiconductor memory with a memory cell, comprising:

a storage capacitor; and

a selection transistor, the selection transistor being formed at a web made of semiconductor material, having a first and a second source/drain region, and at least one gate layer, the web being arranged on an insulation layer, the first source/drain region being arranged on the insulation layer at one lateral end of the web, the second source/drain region being arranged on the insulation layer at another lateral end of the web, the web having two longitudinal sides and a top side, the two longitudinal sides of the web and the top side of the web being covered with a layer sequence, the layer sequence including a gate dielectric and a gate electrode.

2. The semiconductor memory as claimed in claim 1, wherein the storage capacitor is a trench capacitor, the trench capacitor having an inner capacitor electrode and an outer capacitor electrode, the inner capacitor electrode being isolated from the outer capacitor electrode by a capacitor dielectric, the trench capacitor being disposed below the insulation layer, the capacitor dielectric extending as far as the bottom of the storage capacitor.

3. The semiconductor memory as claimed in claim 2, wherein the inner capacitor electrode of the storage capacitor extends as far as a lower side of the insulation layer and is connected by a surface contact to the first source/drain region of the selection transistor.

4. The semiconductor memory as claimed in claim 3, wherein top side of the surface contact for the inner capacitor electrode is arranged below a level of the top side of the web and is electrically insulated from a word line passing the storage capacitor by an insulating upper filling structure.

5. The semiconductor memory as claimed in claim 1, wherein the inner capacitor electrode of the storage capacitor extends as far as a lower side of the insulation layer and is connected by a surface contact to the first source/drain region of the selection transistor.

6. The semiconductor memory as claimed in claim 5, wherein a top side of the surface contact for the inner capacitor electrode is arranged below a level of the top side of the web and is electrically insulated from a word line passing the storage capacitor by an insulating upper filling structure.

7. The semiconductor memory as claimed in claim 1, wherein a semiconductor substrate is doped below the buried insulation layer.

8. The semiconductor memory as claimed in claim 2, wherein a semiconductor substrate is doped below the buried insulation layer.

9. The semiconductor memory as claimed in claim 1, wherein the second source/drain region has, in a longitudinal direction of the web, the same dimension as a lower

side of a spacer of a word line covering the web, and wherein the second source/drain region is connected to a bit line contact on a side remote from the web.

10. The semiconductor memory as claimed in claim 9, wherein a bit line is arranged above the web, the bit line running parallel to a longitudinal direction of the web and is connected to the second source/drain region.

11. The semiconductor memory as claimed in claim 1, wherein a bit line is arranged above the web, the bit line running parallel to a longitudinal direction of the web and is connected to the second source/drain region.

12. The semiconductor memory as claimed in claim 1, wherein a word line runs perpendicular to a longitudinal direction of the web, the word line covering the gate dielectric on both longitudinal sides and on the top side f the web.

13. The semiconductor memory as claimed in claim 1, wherein the semiconductor memory has a plurality of memory cells with selection transistors formed at webs, a bit line contact is arranged at a first predetermined crossover point between a bit line and a word line, and a word line passes above a storage capacitor at a second predetermined crossover points.

14. The semiconductor memory as claimed in claim 13, wherein the first predetermined crossover points are every second crossover point.

15. The semiconductor memory as claimed in claim 14, wherein the second predetermined crossover points are the remaining crossover points.

16. The semiconductor memory as claimed in claim 13, wherein the second predetermined crossover points are the remaining crossover points.

17. The semiconductor memory as claimed in claim 1, wherein the semiconductor memory has a plurality of memory cells with selection transistors formed at webs, a bit line contact is arranged at a first predetermined crossover point between a bit line and a word line, and a word line passes below a storage capacitor at a second predetermined crossover points.

18. The semiconductor memory as claimed in claim 1, wherein the integrated semiconductor memory is a dynamic read-write memory.